

I claim:

- 1    1.    An apparatus, comprising:  
2            a test controller, coupled between a bus and first and second cores in a multi-  
3                        core computer, to operate a data flow stress test in the multi-core  
4                        computer.
- 1    2.    The apparatus of claim 1, wherein the test controller includes:  
2            a first multiplexer coupled between the first core and the bus;  
3            a second multiplexer coupled between the second core and the bus;  
4            a register to store test information; and  
5            a control circuit coupled between the register and the first and second  
6                        multiplexers.
- 1    3.    The apparatus of claim 2, wherein:  
2            the control circuit is to select an input of the first multiplexer between a first  
3                        data request from the first core and a test data request from the control  
4                        circuit.
- 1    4.    The apparatus of claim 2, wherein:  
2            the control circuit is to select an input of the second multiplexer between a first  
3                        data request from the second core and a test data request from the  
4                        control circuit.

1 5. The apparatus of claim 1, wherein:

2 the test controller is to be electrically deactivated after the stress test.

1 6. The apparatus of claim 1, wherein:

2 the test controller, first core, and second core are all disposed on a same  
3 integrated circuit.

1 7. A system comprising:

2 a memory;

3 a multi-core computer coupled to the memory; and

4 a test controller, coupled between a bus and first and second cores in the multi-  
5 core computer, to operate a data flow stress test in the multi-core  
6 computer.

1 8. The system of claim 7, wherein the test controller includes:

2 switching logic to switch the bus between data requests from at least one of the  
3 first and second cores and test data requests from the test controller.

1 9. The system of claim 7, wherein:

2 the test controller includes a register to store test information.

1 10. The system of claim 7, wherein:

2 the test controller is to be electrically deactivated after the stress test.

- 1 11. The system of claim 7, wherein:  
2 the test controller, first core, and second core are all disposed on a same  
3 integrated circuit.
- 1 12. A method comprising:  
2 stress testing a multi-core computer by blocking a first data request from a first  
3 core to a bus and sending a test data request from a test controller to the  
4 bus.
- 1 13. The method of claim 12, wherein:  
2 the stress testing further includes sending a second data request from a second  
3 core to the bus.
- 1 14. The method of claim 12, wherein:  
2 the blocking and the sending are controlled by a test controller.
- 1 15. The method of claim 12, wherein:  
2 the test data request is selected by a test register.
- 1 16. The method of claim 12, wherein:  
2 the stress testing further includes blocking a second data request from a second  
3 core to the bus.

1 17. A machine-readable medium that provides instructions, which when executed  
2 by a set of one or more processors, cause said set of processors to perform operations  
3 comprising:

4 stress testing a multi-core computer by blocking a first data request from a first  
5 core to a bus and sending a test data request from a test controller to the  
6 bus.

1 18. The medium of claim 17, wherein:  
2 the stress testing further includes sending a second data request from a second  
3 core to the bus.

1 19. The medium of claim 17, wherein:  
2 the blocking and the sending are controlled by a test controller.

1 20. The medium of claim 17, wherein:  
2 the test data request is selected by a test register.

1 21. The medium of claim 17, wherein:  
2 stress testing further includes blocking a second data request from a second core  
3 to the bus.

1 22. A machine-readable medium that provides instructions, which when executed  
2 by a set of one or more processors, cause said set of processors to perform operations  
3 comprising:

4 obtaining test data for stress testing a multi-core computer system;

5 writing the test data to a test register in the multi-core computer system through  
6 a test port; and  
7 reading a test result from the test register through the test port.

1 23. The medium of claim 22, wherein:  
2 said writing includes writing an 'on' bit to the test register.

1 25. The medium of claim 22, wherein:  
2 said writing includes specifying data requests to be monitored as triggers to start  
3 a test.

1 26. The medium of claim 22, wherein:  
2 said writing includes specifying test data requests to be issued.